Ex. 7
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Paper 17
Date: September 16, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR PRODUCTS, INC., and
MICRON TECHNOLOGY TEXAS LLC,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00237
Patent 10,268,608 B2

Before JON M. JURGOVAN, NABEEL U. KHAN, and
KARA L. SZPONDOWSKI, *Administrative Patent Judges.*

KHAN, *Administrative Patent Judge*.

DECISION
Denying Petitioner's Request on Rehearing of Decision Denying Institution
of *Inter Partes* Review
35 U.S.C. § 42.71(d)

I. INTRODUCTION

Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC ("Petitioner") filed a Request for Rehearing under 37 C.F.R. § 42.71(d) (Paper 16, ("Request" or "Req. Reh'g")) seeking reconsideration of our decision (Paper 15, ("Decision" or "Dec.")) denying institution of *inter partes* review of claims 1–5 ("the challenged claims") of U.S. Patent No. 10,268,608 B2 ("the '608 patent," Ex. 1001). For the following reasons, Petitioner's Request for Rehearing is denied.

II. STANDARD OF REVIEW

When rehearing a decision on institution, the Board "review[s] the decision for an abuse of discretion." 37 C.F.R. § 42.71(c) (2021). An abuse of discretion may arise if the decision is based on an erroneous interpretation of law, if substantial evidence does not support a factual finding, or if an unreasonable judgment is made in weighing relevant factors. *Star Fruits S.N.C. v. U.S.*, 393 F.3d 1277, 1281 (Fed. Cir. 2005); *Arnold P'ship v. Dudas*, 362 F.3d 1338, 1340 (Fed. Cir. 2004); *In re Gartside*, 203 F.3d 1305, 1315–16 (Fed. Cir. 2000).

Also, 37 C.F.R. § 42.71(d) sets forth, in relevant part that:

> A party dissatisfied with a decision may file a single request for rehearing without prior authorization from the Board. The burden of showing a decision should be modified lies with the party challenging the decision. The request must specifically identify all matters the party believes the Board misapprehended or overlooked, and the place where each matter was previously addressed n a motion, an opposition, a reply, or a sur-reply.

III. ANALYSIS

In our Decision we determined that "claim 1 requires that the data path include two elements: (1) at least one tristate buffer and (2) a delay circuit." Decision 18. After review of the Petition and the evidence of

record we concluded that although Petitioner recognized that claim 1 requires the recited "tristate buffer" to be included in the recited "data path" and, accordingly, provided reasoning why the prior art teaches a data path that includes a tristate buffer, Petitioner did not "state, or otherwise make a showing, that the write and read leveling circuitry [the recited "delay circuit"] are included in" the data path. Decision 19–20.

Petitioner argues now that the Board "overlooked the Petition's explanation of how the '*data paths'* are controlled and its supporting evidence, which show that the data paths include the delay circuit." Req. Reh'g 1. According to Petitioner, the Board focused primarily on limitation 1[j] in the Decision, but that it was the analysis of the preceding limitation 1[i], reciting "a command processing circuit configured to . . . control the data path in accordance with the module control signals and the module clock signal," that contained the information showing how the delay circuitry is included in the data path. Req. Reh'g 1–2; *see also* Req. Reh'g 4 (arguing that the Board "overlooks the Petition's explanation of how Osanai discloses '*a command processing circuit configured to . . . control the data path*' in limitation 1[i] . . . which contained the information the Board suggested was missing.")

Petitioner argues that had we considered the analysis of limitation 1[i], we would have seen the following: (1) that the Petition explained that each buffer circuit has two different data paths for reading and writing operations (Req. Reh'g 5 (citing Pet. 39)); (2) that the Petition stated that certain components, such as selectors 331–334 and input/output terminals 341 and 342 are included in the data paths for read and write operations (Req. Reh'g 6); (3) that the Petition cites paragraph 97 of Osanai which explains that the read and write data paths include FIFO (Write)

circuit 301 and FIFO (Read) circuit 302 (Req. Reh'g 6 (citing Ex. 1005 ¶ 97)); (4) that the components in these data paths, such FIFO (Write) and FIFO (Read) circuits, use local clocks LCLKR and LCLKW (Req. Reh'g 7 (citing Pet. 40)); (5) that LCLKR and LCLKW are used for timing read and write operations (Req. Reh'g 7–8 (citing Ex. 1003 ¶ 122; Ex. 1005 ¶ 93)); (6) that local clocks LCLKR and LCKLW originate from their respective read and write leveling circuitries (Req. Reh'g 8–9 (citing Ex. 1003 ¶¶ 121–122)); (7) that because FIFO (Read) and FIFO (Write) circuits use these local clocks LCLKR and LCLKW, that the data paths include a delay circuit (read and write leveling circuits) (Req. Reh'g 11).

We are unpersuaded by Petitioner's contentions summarized above because they were never made in the Petition and, to the extent that they were, are now newly being reframed to support an argument that was also never made in the Petition. A request for rehearing is not an opportunity to present new arguments.

For example, one of Petitioner's primary assertions above is that Osanai's read and write data paths include a FIFO (Write) and FIFO (Read) circuit. Req. Reh'g 6. The Petition, however, makes no mention of these FIFO circuits.[1] Similarly, Petitioner argues that the FIFO circuits use the local clocks LCKLR and LCKLW. Req. Reh'g 7. This too is not mentioned in the Petition. Neither is Petitoner's contention that the local clocks LCKLR and LCKLW originate from their respective read and write leveling

[1] The FIFO circuits appear only in figures from Osanai reproduced in the Petition. *See e.g.* Pet. 39. Additionally, the FIFO circuits are also not mentioned in Petitioner's expert testimony, other than briefly in the discussion of dependent claims 4 and 5. Ex. 1003 ¶¶ 153, 157.

circuits. Each one of these contentions is crucial because they underpin the chain of inferences Petitioner wants us to draw to reach the conclusion that the data paths include the read and write leveling circuits (the recited "delay circuit").

Rather than demonstrate that these contentions appear in the Petition, Petitioner points us to paragraphs from Osanai that were cited in passing as part of longer string cites used to support contentions in the Petition that are only tangentially related to Petitioner's argument here that the read and write leveling circuits are included in the data path.[2] The same is true for citations to Petitioner's expert testimony, most of which appear in the analysis of limitation 1[j], which Petitioner tacitly acknowledges supports a contention different than that the delay circuit is included in the data path.

As for the assertions that do appear in the analysis of limitation 1[i][3], such assertions are used to support Petitioner's contention that "a POSITA would have recognized that Osanai's data register buffer 300 selects data paths '*in accordance with the module control signals and the module clock signal*,'" not that the data path would include the delay circuitry. Pet. 40. As we explained in our Decision, at no point does Petitioner even assert that

[2] Paragraph 97 of Osanai, for example, is one of several paragraphs that appear in string cites supporting Petitioner's contention that Osanai's data register control circuit selects (and therefore controls) data paths in buffer circuit 300. Pet. 39–40.

[3] The assertions that appear in the relevant portion of the analysis of limitation 1[i] include that the "data register control circuit enables different paths for reading and writing operations" (Pet. 39) and that it "selects (or '*controls*') certain paths using SEL, INB, and OUTB signals as well as selectors 331–334" (Pet. 39) and that "the data path would have used the appropriate clocks [LCLKR and LCLKW] in their respective read/write operation data paths" (Pet. 40).

the data path includes the delay circuitry. Decision 19 ("Petitioner does not, however, state, or otherwise make a showing, that the write and read leveling circuitry are included in any one of the data paths that are relied upon by Petitioner. Nor does Petitioner show how these circuits would be included in the recited data path.")

Ultimately, in order to make the chain of inferences Petitioner sets forth in its Request for Rehearing, we would have to weave together citations and statements supporting a contention different than the one Peitioner now seeks to make, and combine them with contentions that were not made in the Petition at all, to come to the conclusion Petitioner now seeks. That is not our role. Instead it was incumbent upon the Petitioner to set forth the evidence and explain how it demonstrates that the data path includes the delay circuitry. *See* 37 C.F.R. § 42.22(a)(2) (requiring the Petition to contain "a detailed explanation of the significance of the evidence.") Because Petitioner did not do so, we are not persuaded to modify our Decision.

IV. CONCLUSION

For the foregoing reasons, Petitioner has not demonstrated that we abused our discretion in denying institution of *inter partes* review.

V. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Petitioner's Request for Rehearing is *denied*.

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